High level synthesis of a H.246/AVC decoder on FPGA platform

Román Neris Tomé, Antonio Núñez Ordóñez, Pedro Pérez Carballo
SICAD Division
Institute for Applied Microelectronics
Las Palmas de Gran Canaria, Spain
rneris@iuma.ulpgc.es

Abstract—**The traditional design methodology of integrated systems, or SoCs, is not adapted for complex systems, since the increase of the complexity generates problems with very important repercussions. The speed of the technological advances reduces increasingly the designs life. In addition, the system must have a relation cost / features optimized and a high degree of reliability. The global purpose of this work will be the application of design techniques of high level synthesis in a methodology adapted in the video applications domain, particularly in the H.264/AVC decoder design. It will use complex design flows in the hardware domain, which it will allow the synthesis and characterization of the system on a FPGA platform, with the purpose of obtaining a completely characterized system that allows the accomplishment of comparatives and extraction of conclusions after the obtained results. With the obtained results, there will be made comparatives that they reflect the variations of important parameters in any design of these characteristics, such as consumption of resources and frequency.**

High level synthesis, H.264/AVC, FPGA, resources, frequency.

I. INTRODUCTION

Nowadays, the multimedia systems have a great importance in the daily life. It's totally common the use of high quality audio and video players, such as digital cameras, portable DVDs, mobile telephony with videoconference, digital television, etc. It is in this context where the new standards are necessary re appear new standards of codification that look for the available resources optimization [1].

The hardware acceleration is a feasible solution to the possible temporary restrictions of the design. This approach implies the accomplishment of a partition of the application code, dividing in modules, and the design of hardware units to accelerate the critical functions with the highest computational cost [2].

The standard developed by the ISO/IEC MPEG-4 Advanced Video Coding (AVC) and ITU-T H.264 experts set new levels of video quality for a given bit-rate. In fact, H.264 (from this point the standard will be referred only by its ITUT denomination) outperforms previous standards in bit-rate reduction [3].

The main goal of this work will be the high-level synthesis of an H.264/AVC video decoder for a FPGA platform target.

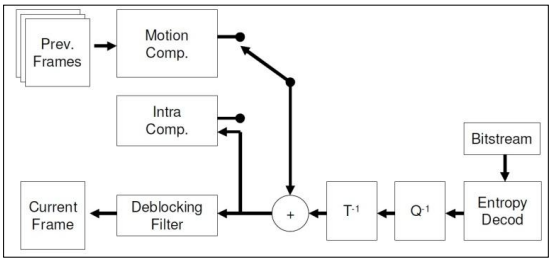

Figure 1. H.264/AVC decoder

A work methodology will be defined starting from an existing SystemC model of the video decoder. The design methodology presented in this work performs the necessary steps to achieve the correct synthesis on a FPGA platform. Finally, the most relevant results will be presented and compared with other works found in the literature.

II. PREVIOUS CONSIDERATIONS

As a starting point, the H.264/AVC decoder has been partitioned in different blocks as is represented in figure 1:

- D_FILTER block (1): includes all the modules responsible for the filtered edges functions.
- INTER_P block (2): as the INTRA_P block, contains the modules of the inter prediction processing flow.
- INTRA_P block (3): includes the necessary modules for the intra prediction. This includes the segmentation of the prediction flow, the preparation of the records for the information storage and the processing of the own elements.
- IQIT block (4): takes charge of the decoded residual information from the CAVLC decoder.
- CAVLD block (5): includes both the CAVLC decoder, and all the modules that take part in the flow of information control phase.

During the design process, a high-level and logical synthesis for each of these blocks separately has been done, which allows to extract information for each of them. Subsequently, the obtained results were compared among them and with the results obtained in other works in the video decoder filed.

III. RESULTS

The obtained results for both synthesis processes are presented in Table 1. The high-level synthesis was performed with *Cadence C-to-Silicon* (a). In the case of the logical synthesis, two different tools were used: *Xilinx Synthesis Tools (XST)* (b) integrated in the *Xilinx PlanAhead* environment and *Synopsys Synplify* (c). The FPGA platform chosen was a Virtex-5 XCV5FX130T [7].

	Est Freq (MHz)			Regs		BRAMs		LUTs		
	(a)	(b)	(c)	(b)	(c)	(b)	(c)	(a)	(b)	(c)
(1)	100,0	109,1	112,2	33.993	9.882	0	3	80.283	22.534	9.550
(2)	100,0	108,3	123,1	66.313	13.249	0	5	116.540	40.343	12.711
(3)	100,0	108,7	122,3	27.550	9.940	0	1	79.055	26.207	20.492
(4)	100,0	97,8	120,1	62.466	7.414	0	0	123.056	38.681	17.454
(5)	100,0	128,7	149,6	44.524	7.750	1	0	127.899	23.804	7.374

Table 1. Obtained results after the synthesis processes

In Figures 2 and 3, these results are showed graphically, comparing the LUTs and registers utilization predicted by the synthesis tools respectively.

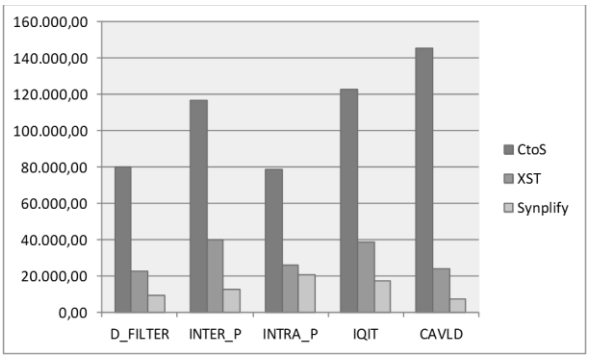

Figure 2. Consumption of LUTs

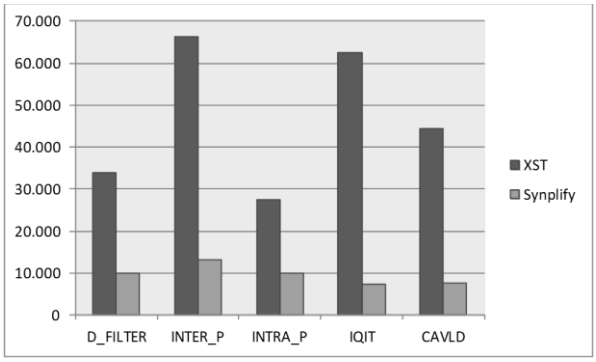

Figure 3. Consumption of registers

IV. COMPARATIVE

Finally, the obtained results were compared with other technical papers. A comparative of maximum frequency and consumption of LUTs are showed in Figure 4 and Figure 5 respectively. The used results were obtained using *Synopsys SynplifyPremier*.

CONCLUSIONS

Is notable the fact that the description of the system at algorithm level is more productive form the designer point of view if the synthesis flow can produce design with good quality of results.

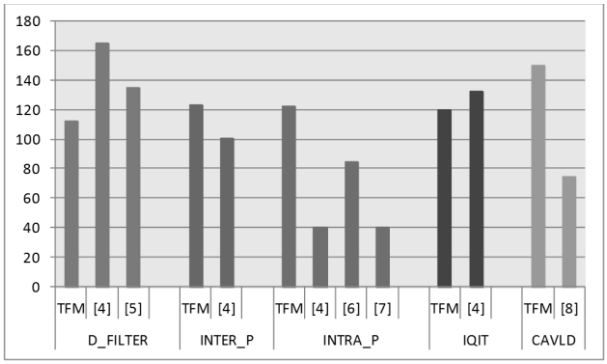

Figure 4. Maximum frequency estimated

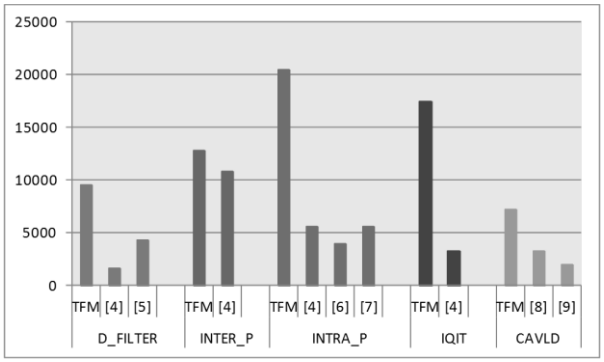

Figure 5. Consumption of LUTs

In this work, we have demonstrated that a H.264/AVC described in SystemC can be synthetized to a FPGA implementation with the same quality of results that the same design done at RTL level. A considerable decrease in the effort (divided by 10) of design is obtained, allowing reduce the time-to-market as well. Therefore, the advantages of this methodology must be considered.

REFERENCES

[1] I. E. G. Richardson, *H.264 and MPEG-4 Video Compression: Video Coding for Next-Generation Multimedia.* John Wiley, 2003.

[2] N. Nedjah and L. de Macedo Mourelle, *Co-Design for System Acceleration: A Quantitative Approach.* Michigan University, 2007.

[3] International Telecommunication Union. ITU-T recommendation H.264: Advanced video coding for generic audiovisual services. 2010.

[4] L. V. Agostini, A. P. Azevedo Filho, V. S. Rosa, E. A. Berriel, T. G. S. Santos, S. Bampi and A. A. Susin. FPGA design of A H.264/AVC main profile decoder for HDTV. Presented at Field Programmable Logic and Applications, 2006. FPL '06. International Conference on. 2006.

[5] V. S. Rosa, A. A. Susin and S. Bampi. An HDTV H.264 deblocking filter in FPGA with RGB video output. Presented at Very Large Scale Integration, 2007. VLSI - SoC 2007. IFIP International Conference on. 2007.

[6] Xun He, Dajiang Zhou, Jinjia Zhou and S. Goto. A new architecture for high performance intra prediction in H.264 decoder. Presented at Intelligent Signal Processing and Communication Systems, 2009. ISPACS 2009. International Symposium on. 2009.

[7] W. T. Staehler, E. A. Berriel, A. A. Susin and S. Bampi. Architecture of an HDTV intraframe predictor for a H.264 decoder. Presented at Very Large Scale Integration, 2006 IFIP International Conference on. 2006.

[8] T. G. George and N. Malmurugan. A new fast architecture for HD H.264 CAVLC multi-syntax decoder and its FPGA implementation. Presented at Conference on Computational Intelligence and Multimedia Applications, 2007. International Conference on. 2007.

[9] T. L. da Silva, J. A. Vortmann, L. V. Agostini, A. A. Susin and S. Bampi. Low cost and memoryless CAVLD architecture for H.264/AVC decoder. Presented at VLSI, 2009. ISVLSI '09. IEEE Computer Society Annual Symposium on. 2009.