Call for applications - PhD candidate

Performance and Safety/Security Management in automotive and IoT applications

Location: TIMA Laboratory (AMfoRS team), Grenoble, France
Funding: 3-year PhD grant, ~1700€/month (brut) – HADES Penta (European) project
Starting date: September 2017
Key-words: hardware safety and reliability, performance monitors, IEEE 1687, test and recovery

Context

For mission and safety-critical systems, such as in space, automotive, healthcare or avionic domains, an early detection of potential troubles is necessary to avoid safety issues and control costs. This solution will be also applicable for cheap IoT ranging from convenience products to near-critical systems.
In order to ensure dependability, one of the first requirements is to be able to efficiently test the devices, after manufacturing (against manufacturing defects) but also throughout their operation lifetime (against e.g., ageing-related defects, but also for detecting malicious attacks). The IEEE 1687-2014 standard, commonly called IJTAG for "Internal JTAG", has provided a framework for hierarchical test of these devices, with inclusion of many types of instruments in order to monitor and optimize their behavior. However, the access to the monitored data must be restricted to authorized actors, so that this information cannot be used in a malicious way.

There is an obvious need of developing a hierarchical test infrastructure for on-line secure measurements within integrated circuits and electronic systems. In turn, these on-line measurements will enable self-testing, enhancing dependability features and, in general, facilitating uninterrupted high performance operation, while guaranteeing security requirements. The HADES project envisions creating added value at system and user levels thanks to the test infrastructure reused for hierarchical on-line tests defined in the corresponding field of the application. To support a broad industrial applicability, we plan to use the IJTAG standard for large digital SoCs and SPI or I2C for smaller digital SoCs or more complex multi cores platforms. This choice will allow for high resource reusability thanks to the flexibility of the standard and its related software environment.
In the context of HADES project (Hierarchy-Aware and secure embedded test infrastructure for Dependability and performance Enhancement of integrated Systems), funded by the Penta European call, the challenge is to provide ambitious solutions to the test challenges both in terms of efficiency and security throughout the system lifetime. The project purpose is to address the following markets: i) machine to machine and connected systems, ii) remote-controlled systems, iii) smart home and mobile phone, iv) safety-critical systems - typically found in the automotive and avionics domains, v) mission-critical systems -such as in space and security applications.

Objectives

The proposed research funded by the HADES project, will be carried out in collaboration with many international industrial and academic actors.

In the context previously mentioned, the main objectives are:

- To include at the design phase a large variety of performance and reliability monitors to provide expected correct functionality and performance face to different harsh environments. Some monitors will be also used to predict the remaining lifetime before potential failures, thus eliminating the need for high and useless design margins (strategy

used today in most of the applications). These monitors will allow coping with safety-critical applications, but also to thousand nodes applications as they aim at eliminating downtime of system adaptation and cope with critical application needs. Because of the high number of potential endpoints, a naïve exhaustive insertion strategy would result in a serious design overcharge and a sensible increase in the backend time. Therefore, Machine Vector Learning will be used to identify critical and meaningful monitor insertion points in the design.

- These monitors will be used also to trigger system parameter adaptation, allowing high performance or low power, upon request.

- Data provided by these monitors will be easily collected by a hierarchical approach, standard communication and bus facilities, and will be used not only for system strategies but also for early on-line diagnosis, and further to that, during on-line testing at the customer site. This will also reduce the time-to-market as corrective (provide data integrity) and secured actions (cut the access to secured operations or denial of service actions) can be taken faster.
- While using the new standardized access to instruments, monitors and the system strategies, there is a clear need to provide security at the hardware level, that is, to avoid exposure to real security threats as vulnerabilities to unauthorized access or usage of a system, threats inside the systems that may endanger safety of life. The security will be included not only to prevent these vulnerabilities but also to avoid leaks and misuse of the stored data on IoT component that may lead to –for instance- economic miss use.

To achieve these goals, it will be necessary to enforce dynamic communication through the test interface to collect data and act accordingly, a setup seldom supported by industrial Test Generation Tools. For this reason, the project will exploit the MAST technology developed in the team and currently in industrialization phase.

Profile: Master degree or equivalent in the area of either Electronic Engineering or Computer Science.

Expected skills

Technical: Digital integrated electronics (digital design, VHDL, CAD tools), C/C++ is a must and scripting a plus. Knowledge about front end/back end, assembly language, machine learning algorithms, data science, etc.
Personal: Determination, perseverance, trustworthiness, autonomy, adaptability, initiative, good communication skills
Languages: English: at least B2 equivalent, excellent reading and writing level, good speaking level. Fluency in French is a plus but it is not mandatory.

About TIMA

TIMA Laboratory is a public joint research laboratory located in Grenoble, France, and held jointly by Institut Polytechnique de Grenoble (Grenoble INP), University Grenoble-Alpes and French National Research Council (CNRS). TIMA is a multinational team of over 100 people, with members and interns from all over the world. The research topics of TIMA cover the specification, design, verification, test, CAD tools and design methods for integrated systems, from analog and digital components on one end of the spectrum, to multiprocessor Systems-on-Chip together with their basic operating system on the other end.
This call is from the AMfoRS team, and targets people motivated by hardware security and test. More information about the team is available at http://tima.imag.fr/tima/en/AMfoRS/AMfoRSoverview.html

Advisors

Main advisors: Lorena Anghel, Professor, AMfoRS team and Michele Portolan, Associate Professor.

The work will be carried out in strong cooperation with the other members of the team contributing to the HADES project, in particular Professor Regis Leveugle, and Paolo Maistri, CNRS Researcher.

To apply, send a mail to mailto:michele.portolan@grenoble-inp.fr, with the following attachments (in English or French):

- Detailed curriculum vitae
- Application letter with clear motivations
- Academic transcripts for the last two years of study
- 2 or 3 recommendations (letters or reference persons with e-mail addresses)